UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,462	06/26/2003	Scott L. Michaelis	200205355-1	3496

22879 7590 09/30/2009

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS, CO 80528

EXAMINER	
DU, THUAN N	

ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
09/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
ipa.mail@hp.com
jessica.l.fusek@hp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SCOTT L. MICHAELIS, GREG ALBRECHT,
RICHARD POWERS, and ANURUPA RAJKUMARI

Appeal 2009-003732
Application 10/606,462
Technology Center 2100

Decided: September 28, 2009

Before LEE E. BARRETT, JOHN A. JEFFERY,
and ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-3, 5-7, 9, 10, and 12-23. The Examiner has indicated that dependent claims 4, 8, and 11 would be allowable if rewritten in independent form (Final Rejection 9). We have jurisdiction under 35 U.S.C. § 6(b). We REVERSE.

STATEMENT OF THE CASE

The Invention

The disclosed invention is related generally to multiple processor computer systems. More particularly, Appellants' invention is directed to a system and method for resetting a plurality of cells of partition. (Spec. 1).

Independent claims 1, 15, and 23 are illustrative:

1. A method for resetting a partition of a multiple partition system, wherein the partition comprises a plurality of processors, the method comprising:

executing, by one processor of the plurality of processors, a reset code from firmware;

building a list of reset register addresses associated with the plurality of processors;

sending an interrupt to the other processors of the plurality of processors;

resetting the other processors by writing a reset code to their associated reset registers; and

resetting the one processor by writing to its associated reset register.

15. A partition of multiple partition computer system comprising:

a plurality of processors;

firmware comprising a reset code that resets a portion of the partition, wherein one processor of the plurality of processors executes the reset code; and

random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion.

23. A computer readable medium having computer program logic recorded thereon for operating a partition of a multiple partition computer system, wherein the partition comprises a plurality of processors, the computer program logic comprising:

means for building a list of reset register addresses associated with the plurality of processors;

means for placing each processor of the plurality of processors into a known state; and

means for resetting the plurality of processors by writing a reset code into their associated reset registers.

The References

The Examiner relies upon the following references as evidence:

Walton	US 7,103,639 B2	Sep. 5, 20006
Harrington	US 2003/0236972 A1	Dec. 25, 2003

Applicant's Admitted Prior Art, Spec. (¶ [0002]) (hereinafter "AAPA").

The Rejections

1. The Examiner rejected claims 15-20 and 23 under 35 U.S.C. §102(b) as anticipated by Walton.
2. The Examiner rejected claims 1-3, 5-7, 9, 10, 12, 13, and 21 under 35 U.S.C. § 103(a) as unpatentable over the combination of Walton and Harrington.[1]

[1] Although the heading of the rejection on page 5 of the Answer indicates that claims 1-13 stand rejected as being unpatentable over the combination

3. The Examiner rejected claim 14 under 35 U.S.C. § 103(a) as unpatentable over the combination of Walton, Harrington, and AAPA.
4. The Examiner rejected claim 22 under 35 U.S.C. § 103(a) as unpatentable over the combination of Walton and AAPA.

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the proffered prima facie case.

FINDINGS OF FACT

In our analysis *infra*, we rely on the following findings of fact (FF):

1. Walton discloses:

> First, the system and method preferably establish CM [cell micro-controllers] 304 in each cell. CM 304 preferably controls a Boot-Inhibit-Bit (BIB). BIB causes

---

of Walton and Harrington, the Examiner does not set forth a specific rejection for dependent claims 4, 8, and 11 under the heading. In the Final Rejection, the Examiner objected to dependent claims 4, 8, and 11 for being dependent upon a rejected base claim and indicated that claims 4, 8, and 11 would be allowable if rewritten in independent form (Final Rejection 9). Therefore, dependent claims 4, 8, and 11 are not before us on appeal.

> the booting up to continue until a particular point. Specifically, all booting activities are performed (memory initialization, I/O initialization, and/or the like) excluding activities related to partition formation while the BIB is set. *Accordingly, this permits the partition forming process to be delayed until service processor module 101 has had the opportunity to communicate an updated complex profile to each CM 304.* Under ordinary circumstances, service processor module 101 will cause CM 304 to release the BIB. However, if CM 304 determines the service processor 101 is unavailable for some reason, CM 304 will perform BIB release automatically.

(Col. 4, ll. 50-63, emphasis added).

2. Walton discloses:

> each CM 304 is connected to or able to communicate with service processor module 101. *Service processor module 101 may communicate information via a data structure, which is referred to as the complex profile, that details to which partition the respective cells belong.* Service processor module 101 preferably communicates this information by distributing the complex profile to the respective cells via communication with each respective CM 304. *The complex profile essentially provides a map or set of instructions defining the partition scheme of complex 100.* In a preferred embodiment, the complex profile comprises a configured set.

(Col. 4, l. 64 through col. 5, l. 8, emphasis added).

3. Walton discloses:

> Service processor module 101 preferably strictly controls the distribution and modification of the complex profile. Now, service processor module 101 places the complex profile on each cell via each CM 304 before BIB release. Also, *each CM 304 preferably caches a previous revision of the complex profile or a discrete number of revisions of the complex profile*. Accordingly, the present system and method preferably monotonically assign a revision identifier with the various versions of the complex profile. Thus, each time that the service processor module updates the complex profile on each CM 304—a new higher valued identifier is assigned to the latest revision.

(Col. 5, ll. 23-34, emphasis added).

4. Walton discloses "[t]he configured set defines which cells are configured to be contained within a given partition. For example, the complex profile may include a data field associating cell 0 with partition 0; a data field associating cell 1 with partition 0; and a data field associating cell 2 with partition 1." (col. 5, 11-15).

INDEPENDENT CLAIM 15

Appellants' Contentions

Regarding independent claim 15, Appellants contend, *inter alia*, that Walton does not disclose a "random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion." (App. Br. 6-7).

The Examiner's Response

Regarding independent claim 15, the Examiner disagrees, as follows:

> Furthermore in claim 15, Walton continues to disclose cell microcontrollers that comprise caches (random access memory) to store a data structure referred to as a complex profile (column 5, lines 23-31). The complex profile is a "map" that is created by a service processor module when the cell is booted or reset (column 4, line 51 thru column 5, line 4). This "map" is a data structure that describes the entire partition complex structure such that all partitions, cells of partitions and the processors of the cells are mapped which inherently necessitates a list associated with the cell (portion of the partition). Therefore, Walton clearly anticipates a *random access memory* (caches of the cell microcontrollers) *that is not affected by the reset code, that stores a list* (map of the complex) *associated with the portion* (cell) that is comprised of multiple processors.

(Ans. 11).

Appellants' Reply Brief Response

In the Reply Brief, Appellants contend the Examiner's finding of inherent anticipation is unsupported by the evidence, as follows:

> In the Examiner's Answer, page 11, the examiner cites Walton, column 5, lines 23-31, referring to a "complex profile". In Walton, column 4, line 67 to column 5, line 22, the complex profile may include a data field associating cell 0 with partition 0, etc., but there is no discussion of addresses, and no discussion of the complex profile being in random access memory that is not affected by the reset code. The examiner states that the complex profile "inherently necessitates a list associated with the cell", and then states that such an

> inherent list must anticipate random access memory not affected by the reset code. Applicant respectfully submits that by the examiner's own characterization of a list, there is no necessity for such a list to include addresses, as opposed to mere associations as described in Walton at column 5, lines 13-15. In addition, a list of associations does not require random access memory that is not affected by the reset code (again, Walton is only describing partition formation).

(Reply Br. 2, emphasis in original).

ISSUE 1 (Independent claim 15)

1. Have Appellants shown the Examiner erred in finding that Walton discloses a "random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion?" (Claim 15).

ANALYSIS – ISSUE 1

§ 102 rejection of Independent claim 15

We decide the question as to whether Appellants have shown the Examiner erred in finding that Walton discloses a "random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion." (Claim 15).

We begin our analysis by noting that the Examiner reads the claimed "random access memory" on a "cache within CM 304." (Ans. 4, second sentence). We find Walton discloses that "*each CM* [cell micro-controller] *304 preferably caches a previous revision of*

the complex profile or a discrete number of revisions of the complex profile." (FF 3). Thus, we agree with the Examiner that each CM 304 has an associated cache memory that stores the complex profile.

The Examiner finds Walton's complex profile is a "'map' [that] is a data structure that describes the entire partition complex structure such that all partitions, cells of partitions and the processors of the cells are mapped which *inherently necessitates a list associated with the cell (portion of the partition)*. (Ans. 11, emphasis added).

We agree with the Examiner that Walton describes the complex profile as a map (according to at least one embodiment): "*The complex profile essentially provides a map or set of instructions defining the partition scheme of complex 100.* In a preferred embodiment, the complex profile comprises a configured set." (FF 2).

However, Appellants aver that "[e]ven if each complex characterization [profile] stored a list of all the cells in a partition, *this is not equivalent to a list of addresses associated with a portion of a partition being reset as required by claim 15*." (Brief 7, emphasis added).

In the Reply Brief, Appellants further explain that "[i]n Walton, column 4, line 67 to column 5, line 22, the complex profile may include a data field associating cell 0 with partition 0, etc., but there is no discussion of addresses, and no discussion of the complex profile being in random access memory that is not affected by the reset code." (Reply Br. 2, emphasis in original; *see also* FF 4).

Based upon our review of the evidence, we find that to affirm the Examiner on this point would require speculation on our part. It is our view that the Examiner has not sufficiently developed the record to clearly

establish that Walton's mapping (complex profile) is inherently (i.e., necessarily) a list of addresses stored on a random access memory that is not affected by the reset code where the addresses are associated with the portion of the partition that is reset, as required by the argued portion of independent claim 15. We decline to engage in speculation. We note that "[i]nherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745, (Fed. Cir. 1999).

This reasoning is applicable here. Accordingly, we reverse the Examiner's rejection of independent claim 15 as being anticipated by Walton.

INDEPENDENT CLAIM 23

Appellants' Contentions

Regarding independent claim 23, Appellants contend, *inter alia*, that Walton does not describe means for building a list of reset registers (App. Br. 9).

The Examiner's Response

The Examiner disagrees. The Examiner proffers that "[t]he 'map' of the complex (complex profile) *inherently necessitates* storing addresses of the reset registers since this structure description is used to know the locations via the map." (Ans. 12, ¶ 2, last sentence, emphasis added). In support, the Examiner specifically points to Walton at col. 2, lines 7-15 and column 4, line 47, through column 5, line 34. (Ans. 4-5).

Appellants' Reply Brief Response

Appellants respond that "there is no necessity for such a list to include addresses, as opposed to mere associations as described in Walton at column 5, lines 13-15. (Reply Br. 3, ¶1).

ISSUE 2 (Independent claim 23)

2. Have Appellants shown the Examiner erred in finding that Walton discloses a "means for building a list of reset registers?" (Claim 23).

ANALYSIS – ISSUE 2

§ 102 Rejection of Independent Claim 23

We decide the question as to whether Appellants have shown the Examiner erred in finding that Walton discloses a "means for building a list of reset registers." (Claim 23).

Based upon our review of the record, we find the weight of the evidence supports the Appellants' position. Once again, we find that the Examiner's determination of inherent anticipation is not fully developed in the record and is unsupported by specific evidence.

As previously discussed, Walton discloses "*The complex profile essentially provides a map or set of instructions defining the partition scheme of complex 100.* In a preferred embodiment, the complex profile comprises a configured set." (FF 2). We find nothing in the portions of Walton pointed to by the Examiner (or elsewhere in Walton) that *necessitates* building a list of reset register addresses, as proffered by the Examiner. Even though the Examiner reads the "list of reset register

addresses" on Walton's complex profile (Ans. 12), we also find that Walton's Boot-Inhibit-Bit (BIB) (controlled by CM 304) is not reasonably a "list of reset register addresses," as claimed (claim 23; *see also* FF 1).

Moreover, we note that processors can also be reset by hardware means, such as by applying a particular voltage (e.g., a falling edge) to a dedicated processor reset pin. We also agree with Appellants that "there is no necessity for such a list [complex profile] to include addresses, as opposed to mere associations as described in Walton at column 5, lines 13-15. (Reply Br. 3, ¶1; *see also* FF 4).

Because we find Appellants have met the burden of showing error in the Examiner's prima facie case of anticipation, we reverse the Examiner's rejection of independent claim 23 as being anticipated by Walton.

INDEPENDENT CLAIM 1 (rejected under § 103)

Independent claim 1 stands rejected under § 103 as being unpatentable over the combination of Walton and Harrington. Similar to claim 23, we note that independent claim 1 recites the limitation of "building a list of reset register addresses associated with the plurality of processors." Based upon our review of the record, the Examiner has not established, and we do not find, that Harrington overcomes the deficiencies of Walton previously discussed regarding independent claim 23. Accordingly, we reverse the Examiner's rejection of independent claim 1 as being unpatentable over the combination of Walton and Harrington for the same reasons discussed *supra* regarding claim 23.

Remaining dependent claims

Because we have reversed the Examiner's rejection of each independent claim on appeal, we also reverse the Examiner's rejections of the dependent claims on appeal.

CONCLUSIONS

1. Appellant has established the Examiner erred in rejecting claims 15-20 and 23 under 35 U.S.C. §102(b) as being anticipated by Walton.
2. Appellant has established the Examiner erred in rejecting claims 1-3, 5-7, 9, 10, 12, 13, and 21 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Walton and Harrington.
3. Appellant has established the Examiner erred in rejecting claim 14 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Walton, Harrington, and AAPA.
4. Appellant has established the Examiner erred in rejecting claim 22 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Walton and AAPA.

DECISION

We reverse the Examiner's decision rejecting claims 1-3, 5-7, 9, 10, and 12-23.

REVERSED

pgc

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS CO 80528